REMARKS

In the Final Office Action, Claims 1-26 are pending, were examined and stand rejected. In this Response, Claims 1, 3-7, 9-13, 15, 17, and 21-26 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-26 in view of the following remarks.

I. Double Patenting Rejection

Claims 1 and 2 are provisionally rejected under the obviousness-type double patenting as being unpatentable over Claim 16 of co-pending U.S. Patent Application No. 10/781,512 in view of U.S. Patent No. 6,158,018 to Bernasconi et al. ("Bernasconi"). Applicants hold in abeyance this rejection until such time as the claims on which the rejection is premised are granted.

II. Claims Rejected Under 35 U.S.C. §102(b)

The Examiner has rejected Claims 1-26 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2004/0128590 issued to Derr ("Derr"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim feature, which is neither disclosed, taught nor suggested by Derr:

> 1. A system comprising:
>
> trigger-matching logic to capture an incoming read/write request cycle from a requesting device and to determine if the captured incoming read/write request cycle matches at least one trigger condition of one or more of trigger conditions; and
>
> control logic coupled to the trigger-matching logic to select at least one single instruction upon detection of the at least one matched trigger condition and to execute one or more operations specified by the selected single instruction to modify the captured incoming read/write request cycle prior to transmission to a designated end-device, wherein the single instruction is selected based on the at least one matched trigger condition and the requesting device is different from the designated end-device. (Emphasis added.)

Derr is generally directed to a patch mechanism that can be programmed by software to detect and repair a wide range of conditions such that when a matched recondition is detected, the control logic replaces and/or modifies the sample cycles with a sequence of instructions in the patch buffer to avoid or correct the condition. (See Abstract.) In contrast with Claim 1, Derr does not disclose or suggest control logic coupled to trigger matching logic to select at least one single instruction upon detection of at least one matched trigger condition and to execute one or more operations specified by the single instruction to modify the captured incoming read/write request cycle prior to transmission to a designated end-device, as in Claim 1. Derr does disclose software programmability features that facilitate hardware bug work around by replacing or modified the sampled cycle with the sequence of instructions in the patch buffer to avoid the condition (see page 1, para. 8 and page 4, para. 39), however, that is something completely different from control logic coupled to a trigger matching logic to select a single instruction upon detection of at least one matched trigger condition and to execute one or more operations specified by the selected single instruction to modify the captured incoming read/write request cycle prior to transmission to a designated end-device, as in Claim 1.

Furthermore, in contrast with Claim 1, Derr does not disclose or suggest that the single instruction is selected based on at least one matched trigger condition and the requesting device is different from the designated end-device, as in Claim 1. We submit that neither the sections referred to by the Examiner nor any other disclosure in Derr discloses or suggests control logic to select a single instruction upon detection of at least one matched trigger condition and to execute one or more operations specified by the selected single instruction to modify the captured incoming read/write request cycle prior to transmission to a designated end-device, much less that the single instruction is selected based on the at least one matched trigger condition and the requesting device is different from the designated end-device, as in Claim 1.

For each of the above reasons, therefore, Claim 1, and all claims which depend from Claim 1, are patentable over the cited art.

Each of Applicant's other independent claims include features similar to those highlighted above in Claim 1. Therefore, all of Applicant's other independent claims, and all claims which depend on them, are patentable over the cited art for similar reasons.

Consequently, we request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 1-26.

III. Claims Rejected Under 35 U.S.C. §103

Claims 1-19 and 21-26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bernasconi in view of U.S. Patent Publication No. 2005/0015760 issued to Ivanov et al. ("Ivanov"). Applicant respectfully disagrees with the Examiner's assertions and characterizations of the cited references and therefore traverse this rejection.

Claim 1 recites:

> 1. A system comprising:
> trigger-matching logic to capture an incoming read/write request cycle from a requesting device and to determine if the captured incoming read/write request cycle matches at least one trigger condition of one or more of trigger conditions; and
> control logic coupled to the trigger-matching logic to select at least one single instruction upon detection of the at least one matched trigger condition and to execute one or more operations specified by the selected single instruction to modify the captured incoming read/write request cycle prior to transmission to a designated end-device, wherein the set of instructions is selected based on the at least one matched trigger condition and the requesting device is different from the designated end-device.

Though Applicants argument here is directed to the cited combination of references, it is first necessary to consider their individual teachings to ascertain what combination, if any, can be made from the above cited references.

Bernasconi is generally directed to an integrated circuit including patching circuitry to bypass portions of an incrementally flawed read only memory, where an embedded patching circuitry supplies data stored in flawless portions of the ROM to the DSP until the current DSP program address matches a break address indicating that the next portion of the embedded ROM is flawed. (See Abstract.) In contrast with Claim 1, Bernasconi does not disclose or suggest capture of an incoming read/write request cycle from a requesting device, much less determining whether the captured incoming read/write request cycle matches at least one trigger condition of one or more trigger conditions, as in Claim 1. Bernasconi does disclose the use of a current DSP program address provided by bus 24 from DSP 16 to patching circuitry 22, ROM 18, and RAM

18, such that the DSP program address is compared against a break address to identify flawed DPS program software (see col. 9, lines 53-57 and col. 6, lines 15-23), however, that is something completely different from the capture of an incoming read/write request cycle from a requesting device to determine if the captured incoming read/write request cycle matches at least one trigger condition of one or more trigger conditions, as in Claim 1.

Furthermore, in contrast with Claim 1, Bernasconi does not disclose or suggest trigger matching logic to select at least one single instruction upon detection of at least one match trigger condition and to execute one or more operations specified by the selected single instruction to modify the captured incoming read/write request cycle prior to transmission to a designated end-device, as in Claim 1. We submit that the illustration of the DSP program address coming from the DSP 16 device as well as FIG. 1's illustration of the DSP programming address going to the DSP 16 shown in FIG. 1 of Bernasconi neither disclose or suggest the capture of the incoming read/write request cycle from a requesting device nor transmission to a designated end-device of the modified captured incoming read/write request cycle, as in Claim 1.

As correctly recognized by the Examiner, Bernasconi fails to disclose or suggest that the requesting device is different from the designated end-device, as in Claim 1. As a result, the Examiner cites Ivanov.

Ivanov is generally directed to automatic detection and patching of vulnerable files through the use of binary signatures that have been associated with discovered security vulnerabilities to enable the production of regression-free fixes for security vulnerabilities in binary files. (See Abstract.) We submit that the Examiner's citing of Ivanov fails to rectify the deficiencies of Bernasconi in failing to teach or suggest the capture of an incoming read/write request cycle from a requesting device and the modification of the captured incoming read/write request cycle prior to transmission to a designated end-device, as in Claim 1.

We submit that since the disclosure of Bernasconi is expressly limited to bypassing portions of an internally flawed read only memory. (See col. 6, lines 15-23 and col. 9, lines 53-57.) Hence, no combination of Bernasconi in view of Ivanov can teach or suggest the capture of an incoming read/write request cycle from a requesting device, much less that such incoming

read/write request cycle is modified according to operations indicated by a single instruction prior to transmission to a designated end-device, as in Claim 1. Furthermore, no combination of Bernasconi in view of Ivanov can teach or suggest that the requesting device is different from the designated end-device, as in Claim 1.

For each of the above reasons, therefore, Claim 1, and all claims which depend from Claim 1, are patentable over the cited prior art combination of references to Bernasconi and Ivanov as well as the references of record.

Each of Applicant's other independent claims include features similar to those highlighted above in Claim 1. Therefore, all of Applicant's other independent claims, and all claims which depend on them, are patentable over the cited art for similar reasons. Consequently, we request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1-19 and 21-26.

Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bernasconi in view of Ivanov and further in view of U.S. Patent No. 5,966,547 issued to Hagen et al. ("Hagen"). Applicant respectfully disagrees with the Examiner's assertions and characterizations of the cited references and therefore traverse this rejection.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of each claim or as waiving any argument regarding that claim.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 10/26/07

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CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 10/26/07
Elaine Kwak Date